Electronics5

Lecture 1

Dr. Rania Fouad Ahmed

Administrative rules

- Lecture : Sunday (4st slot), 1:00-3:00
- Teaching assistant: Eng. Shymaa Emad
- Grading Policy
- Assignments: 5
- Quizzes: 10
- Mid term exam: 20
- Oral exam: 15
- Final exam: 75

Course schedule

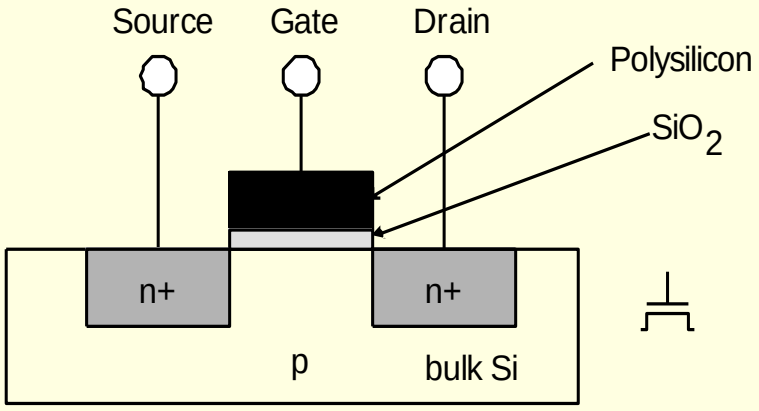
date	subject
29/9/2024 (week 1)	Lecture 1 introduction to VLSI
13/10/2024 (week 3)	Lecture 2 inverter switching characteristics
20/10/2024 (week 4)	Lecture 3 combinational logic circuits
27/10/2024 (week 5)	Lecture 4 delay
3/11/2024 (week 6)	Lecture 5 delay (Cont.)
10/11/2024 (week 7)	Lecture 6 power
17/11/2024 (week 8)	Midterm
24/11/2024 (week 9)	Lecture 7 interconnects
1/12/2024 (week 10)	Lecture 8 interconnects (Cont.)
8/12/2024 (week 11)	Lecture 9 Sequential circuits
15/12/2024 (week 12)	Lecture 10 Dynamic circuits
22/12/2024 (week 13)	Lecture 11 review

Outline

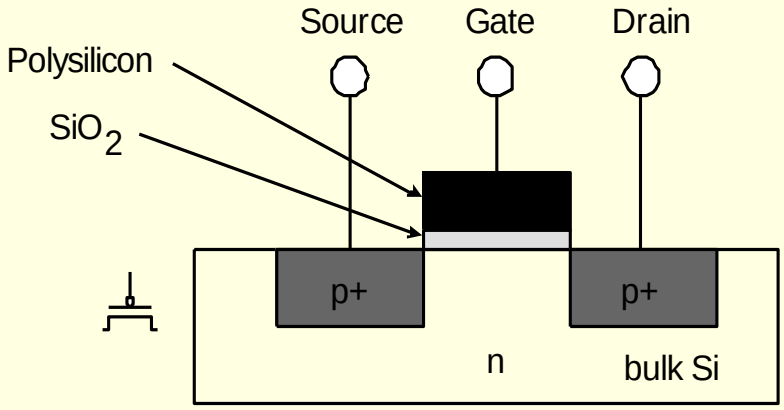
- Operation of MOS Transistors
- CMOS circuits
- CMOS Gate Design
- Pass Transistors
- Transmission Gates

MOS Transistors

- Four terminal device: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors (body is also called the substrate)
  - SiO_2 (oxide) is a “good” insulator (separates the gate from the body
  - Called metal–oxide–semiconductor (MOS) capacitor, even though gate is mostly made of poly-crystalline silicon (polysilicon)



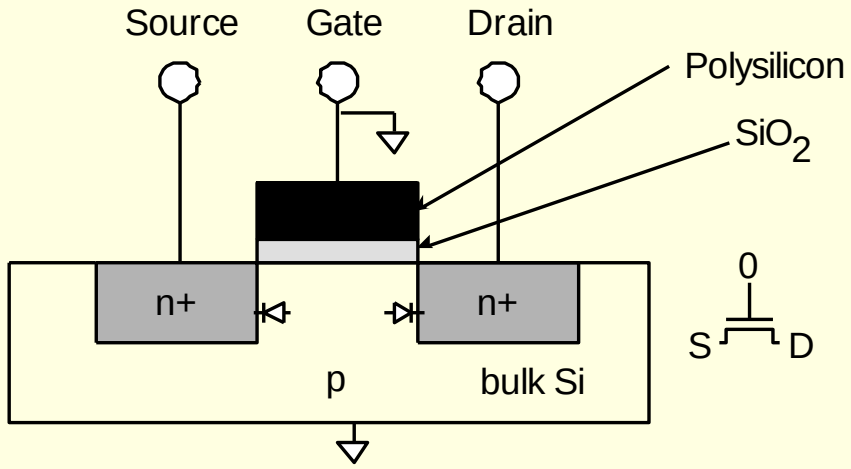
NMOS



PMOS

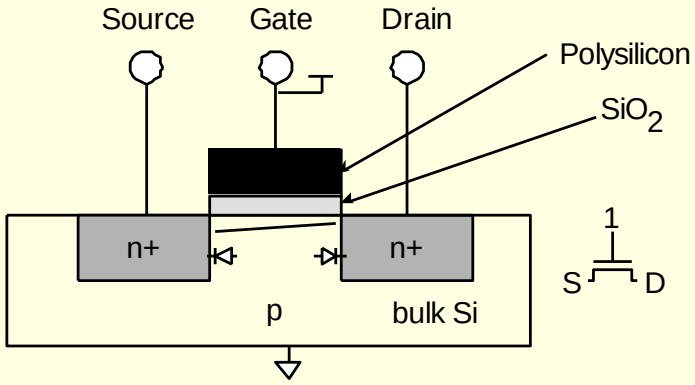
NMOS Operation

- Body is commonly tied to ground (0 V)
- Drain is at a higher voltage than Source
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body “diodes” are OFF
  - No current flows, transistor is OFF



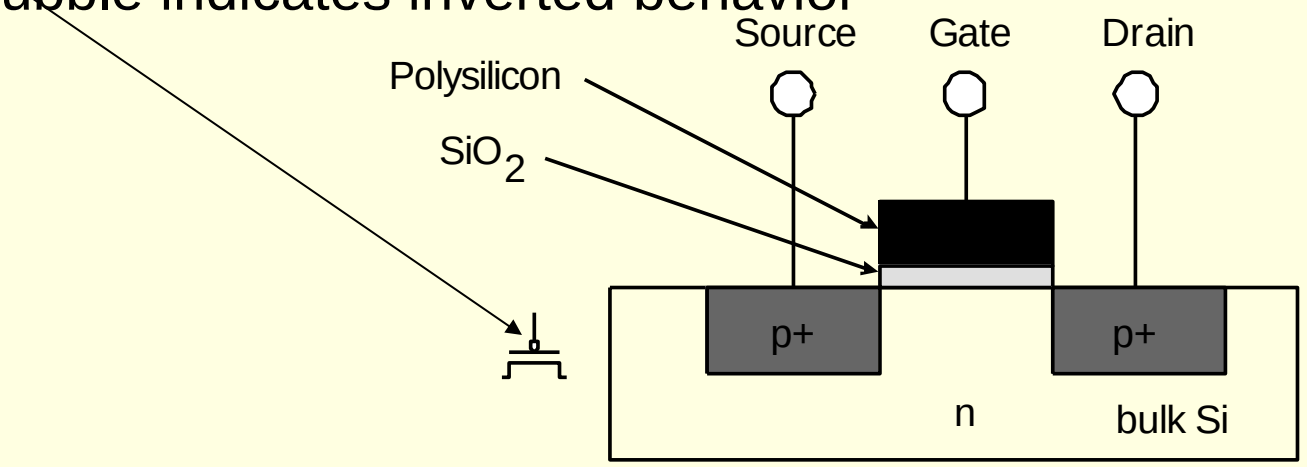
NMOS Operation Cont.

- When the gate is at a high voltage: Positive charge on gate of MOS capacitor
  - Negative charge is attracted to body under the gate
  - Inverts a channel under gate to “n-type” (N-channel, hence called the NMOS) if the gate voltage is above a threshold voltage (VT)
  - Now current can flow through “n-type” silicon from source through channel to drain, transistor is ON



PMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Drain is at a lower voltage than the Source
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

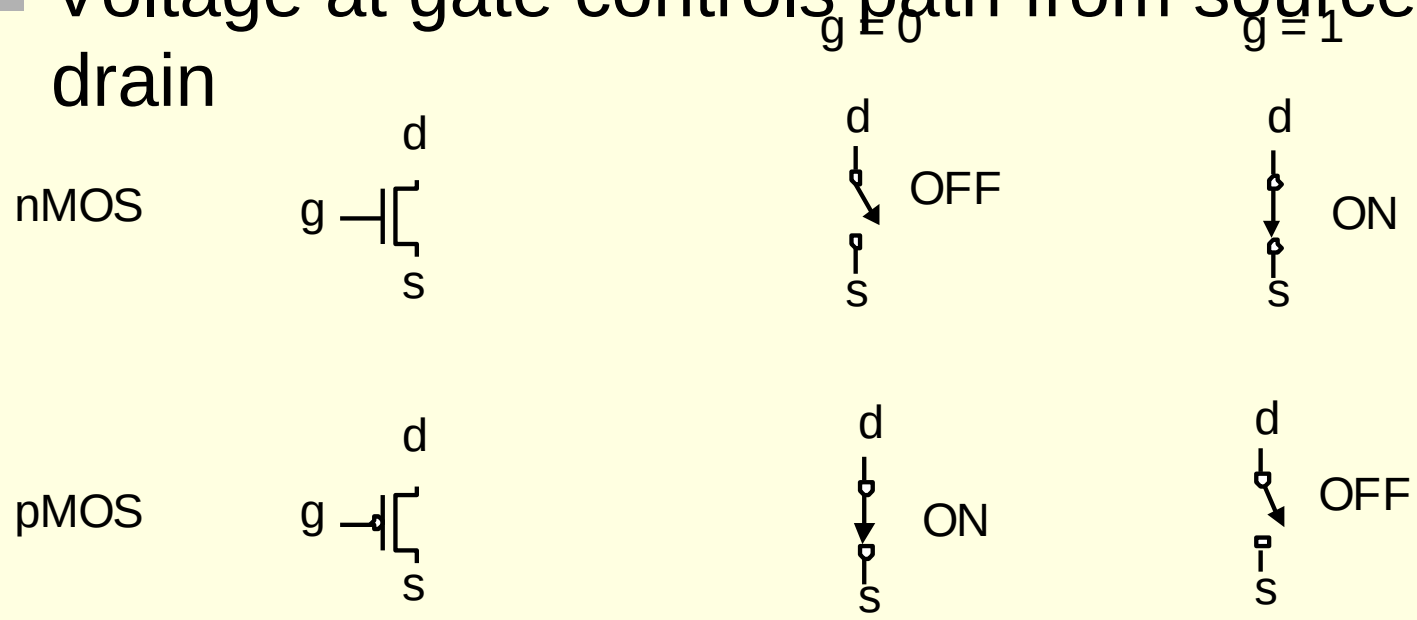


Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0,

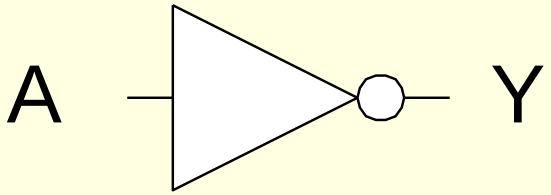
Transistors as Switches

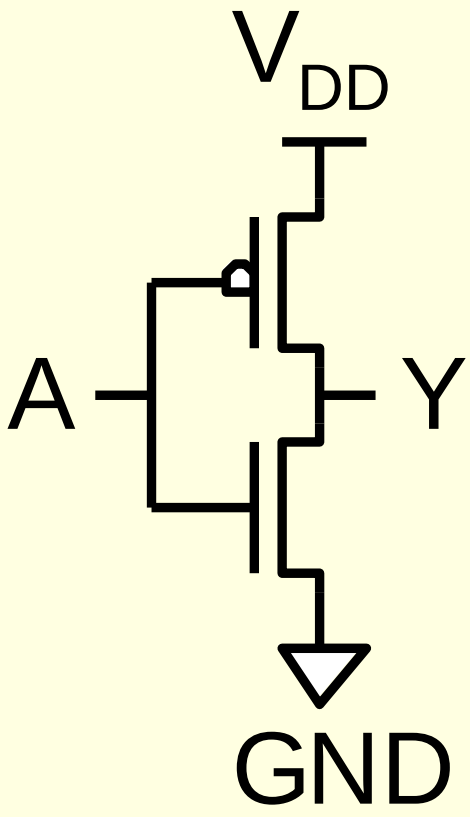
- In Digital circuits, MOS transistors are electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

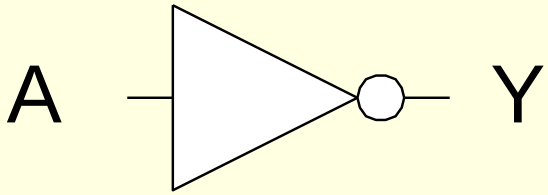
A	Y
0	
1	

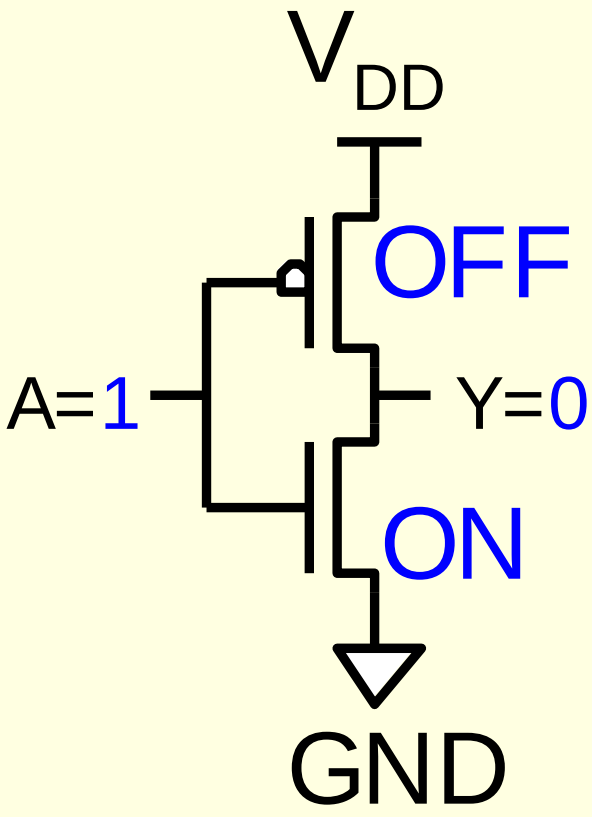




CMOS Inverter

A	Y
0	
1	**0**

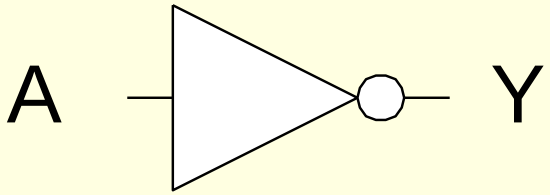


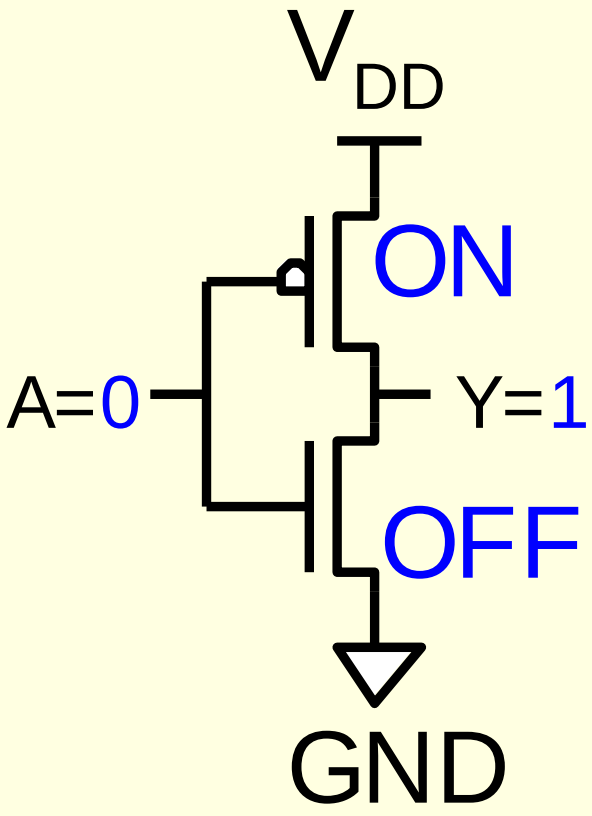


Y is pulled low by the turned on NMOS Device. Hence NMOS is the pull-down device.

CMOS Inverter

A	Y
0	**1**
1	0

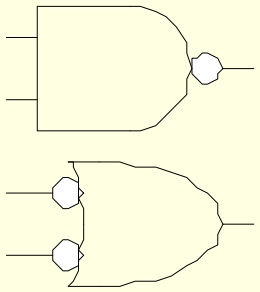


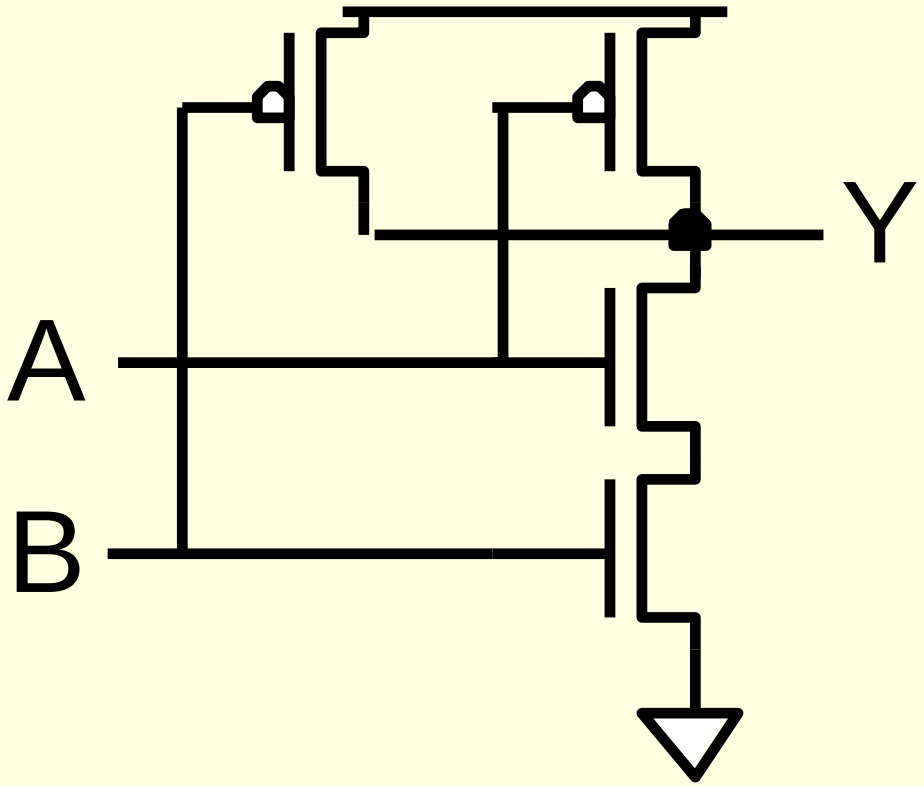


Y is pulled high by the turned on PMOS Device. Hence PMOS is the pull-up device.

CMOS NAND Gate

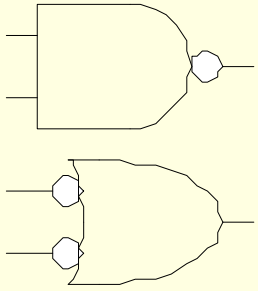
A	B	Y
0	0	
0	1	
1	0	
1	1	

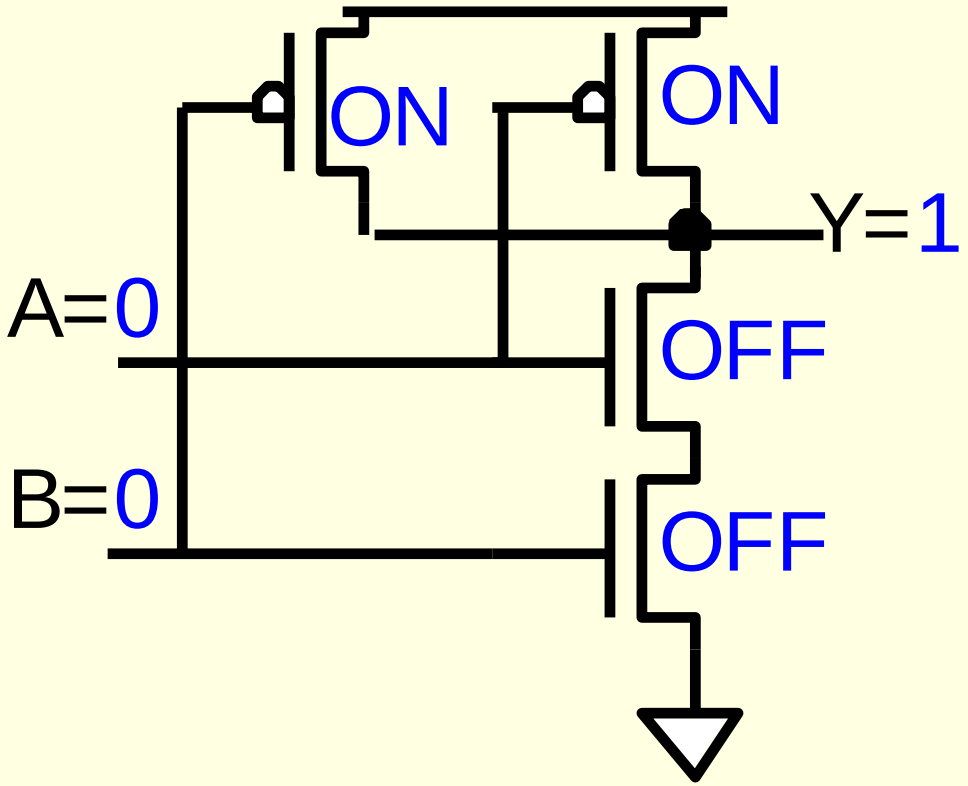




CMOS NAND Gate

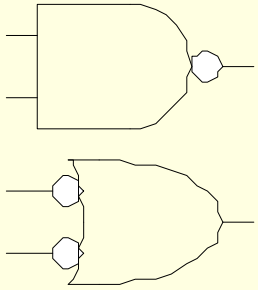
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

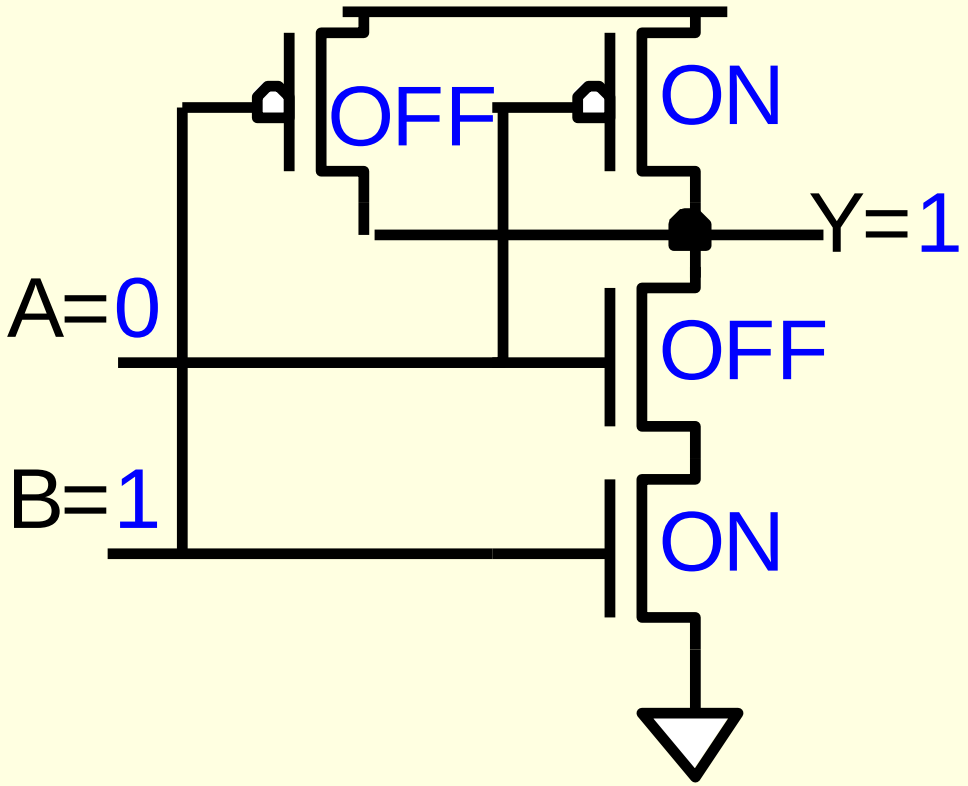




CMOS NAND Gate

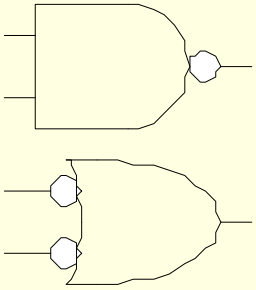
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

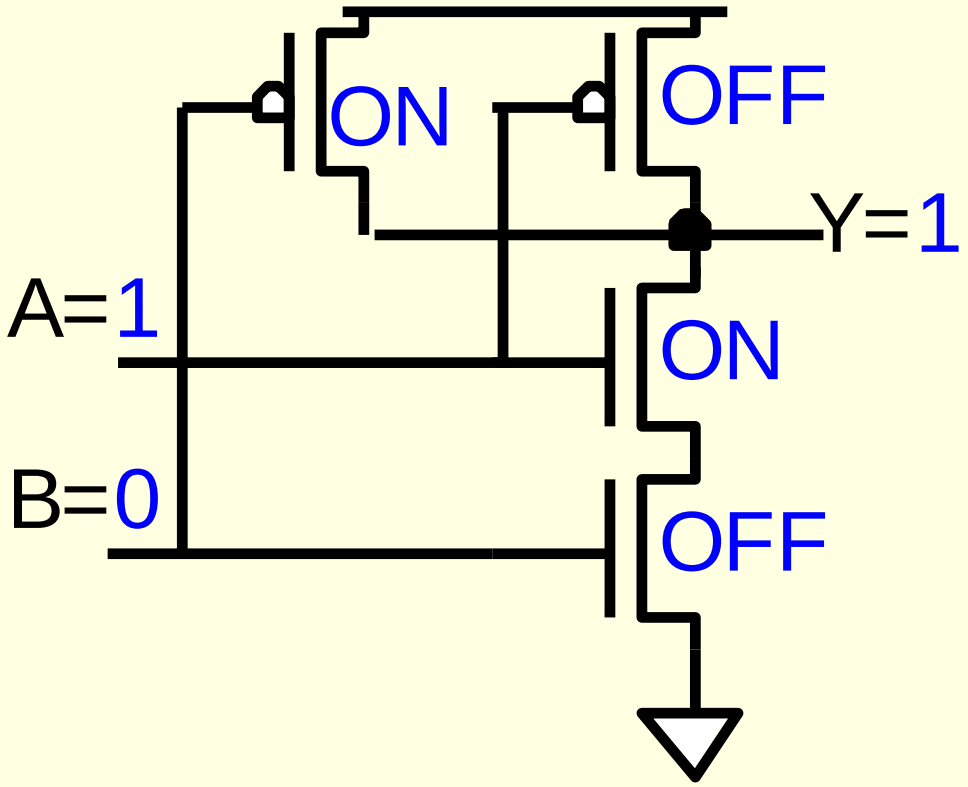




CMOS NAND Gate

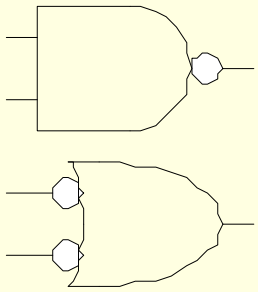
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

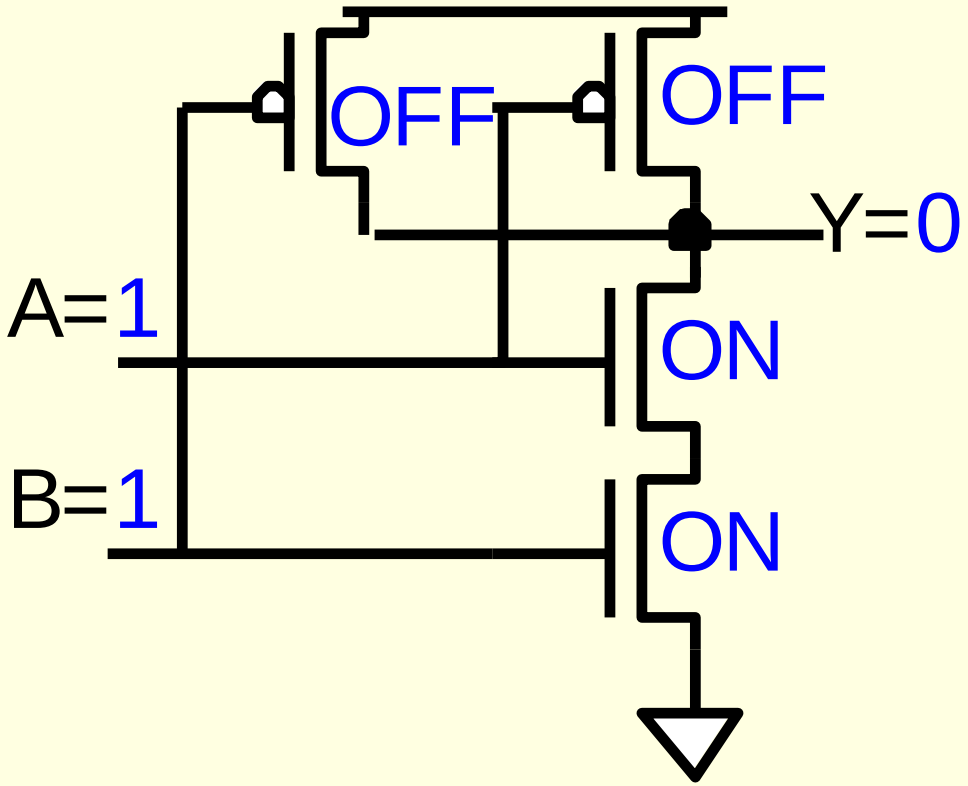




CMOS NAND Gate

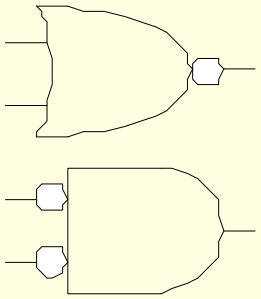
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

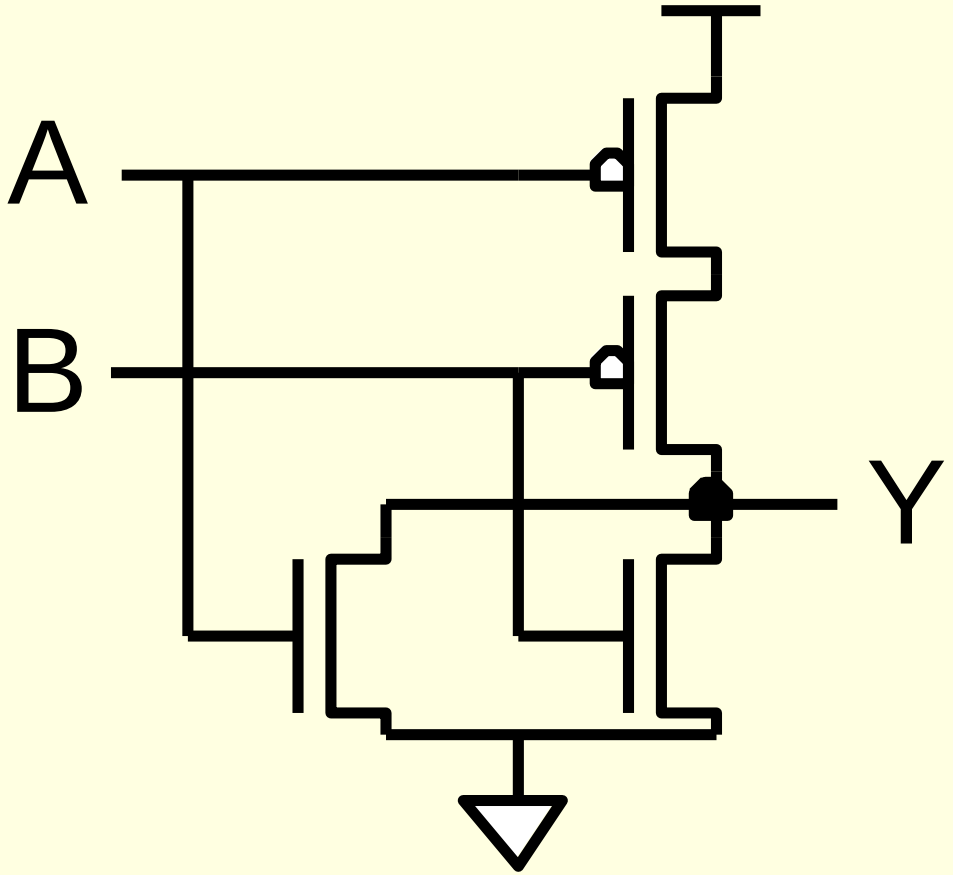




CMOS NOR Gate

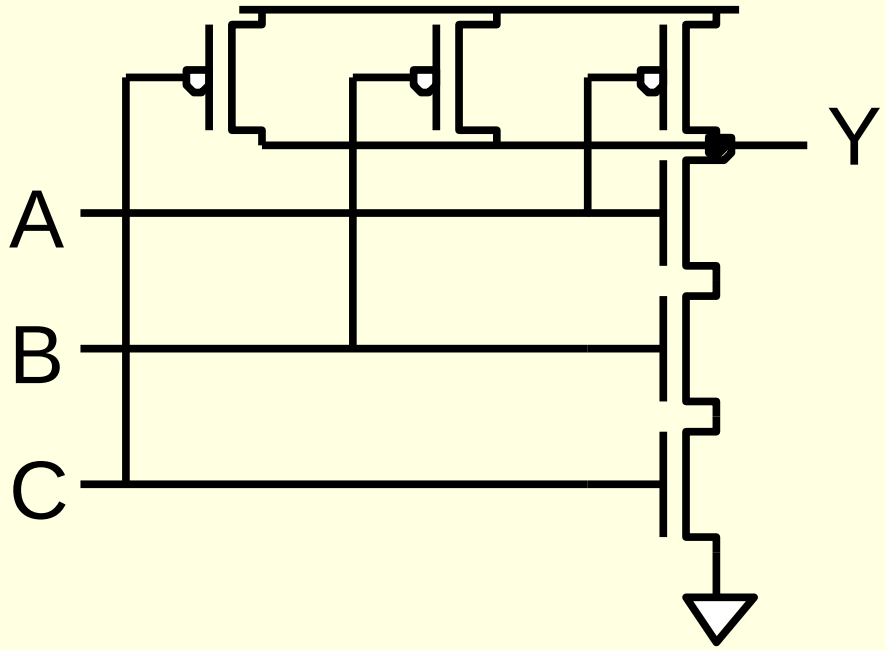
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





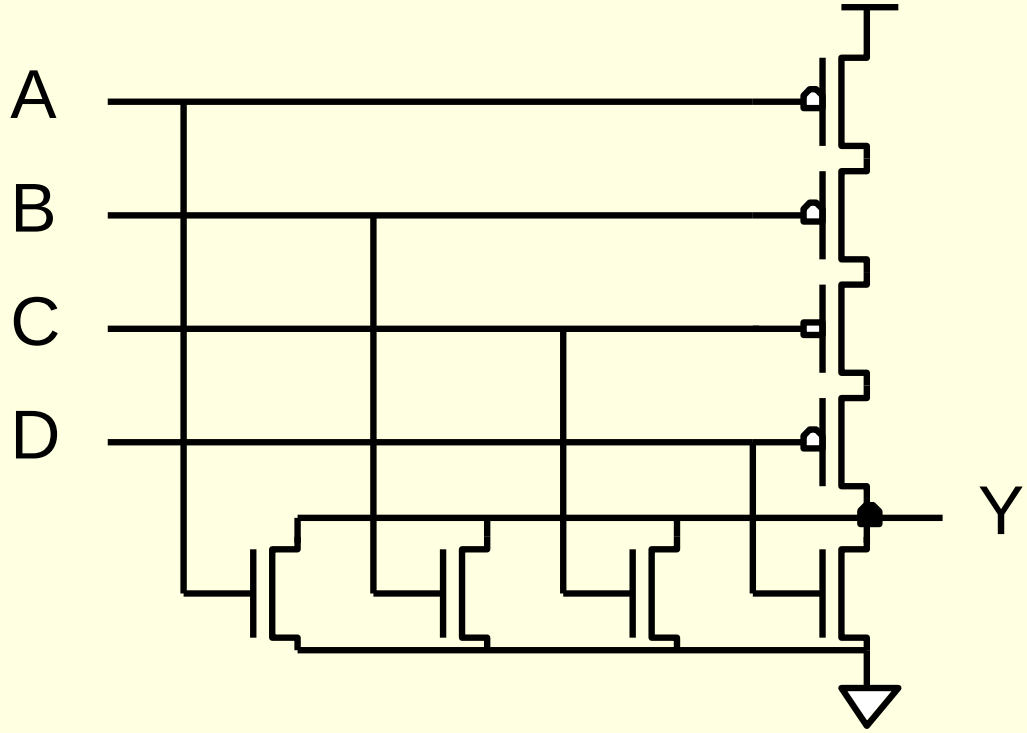
3-input NAND Gate

- Y is pulled low if ALL inputs are 1
- Y is pulled high if ANY input is 0



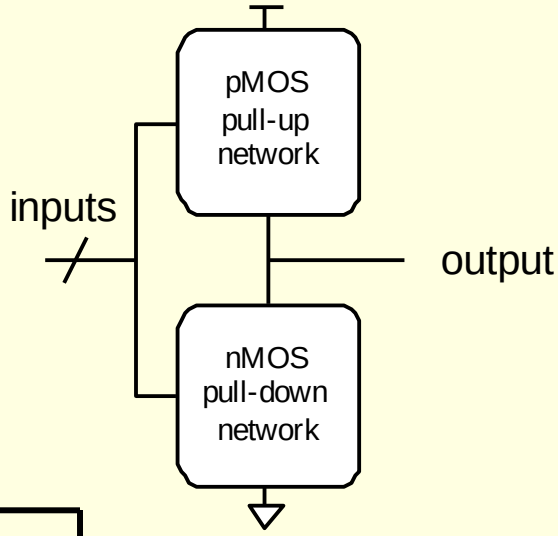
CMOS Gate Design

- A 4-input CMOS NOR gate



Complementary CMOS

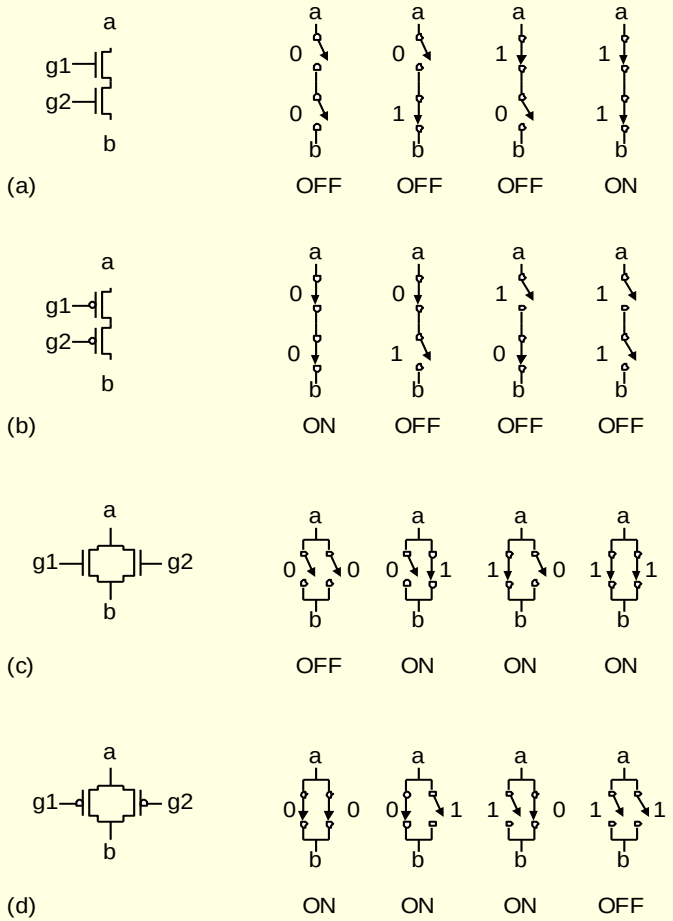
- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

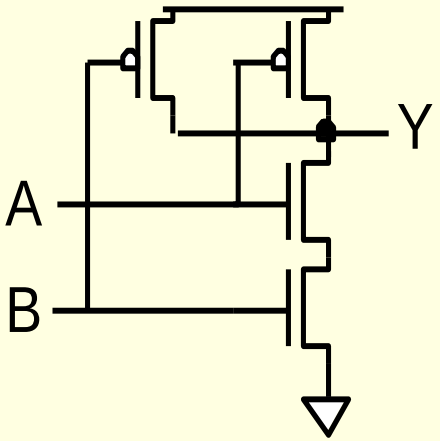
Series and Parallel

- nMOS: 1 = ON
- pMOS: 0 = ON
- *Series*: both must be ON
- *Parallel*: either can be ON



Conduction Complement

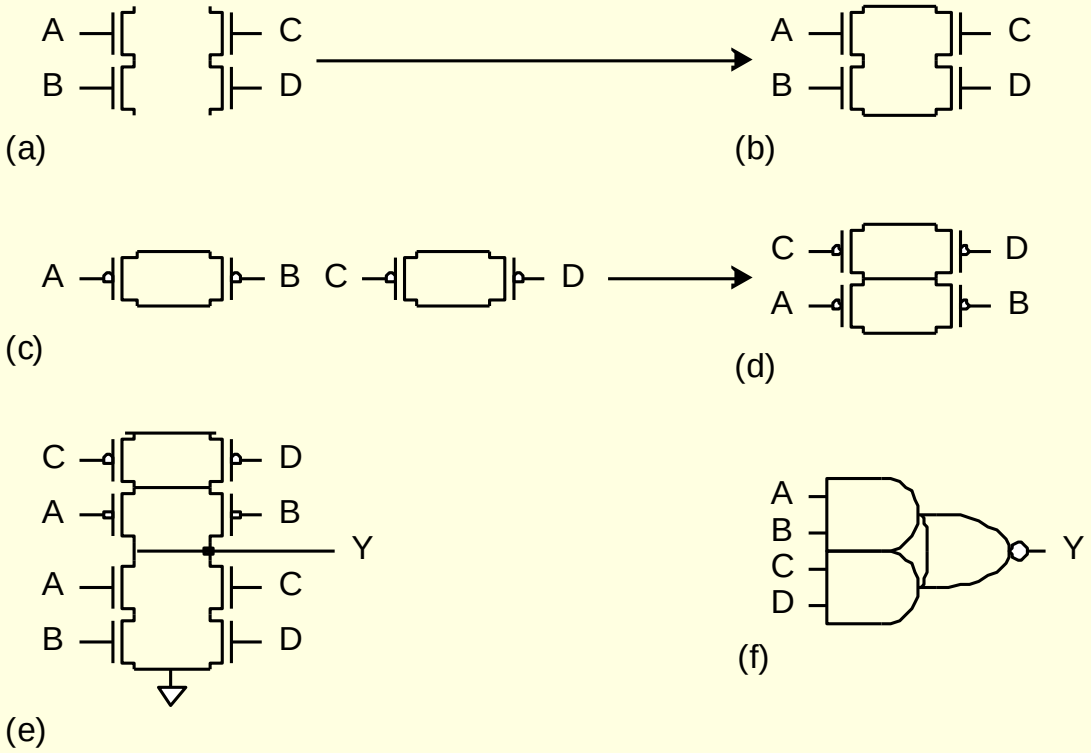
- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate
  - Series nMOS: Y=0 when both inputs are 1
  - Thus Y=1 when either input is 0
  - Requires parallel pMOS



- Rule of *Conduction Complements*
  - Pull-up network is complement of pull-down
  - Parallel -> series, series -> parallel

Compound Gates

- *Compound gates* can do any inverting function
- Ex: AND-AND-OR-INV (AOI22) $Y = \overline{(A \bullet B) + (C \bullet D)}$

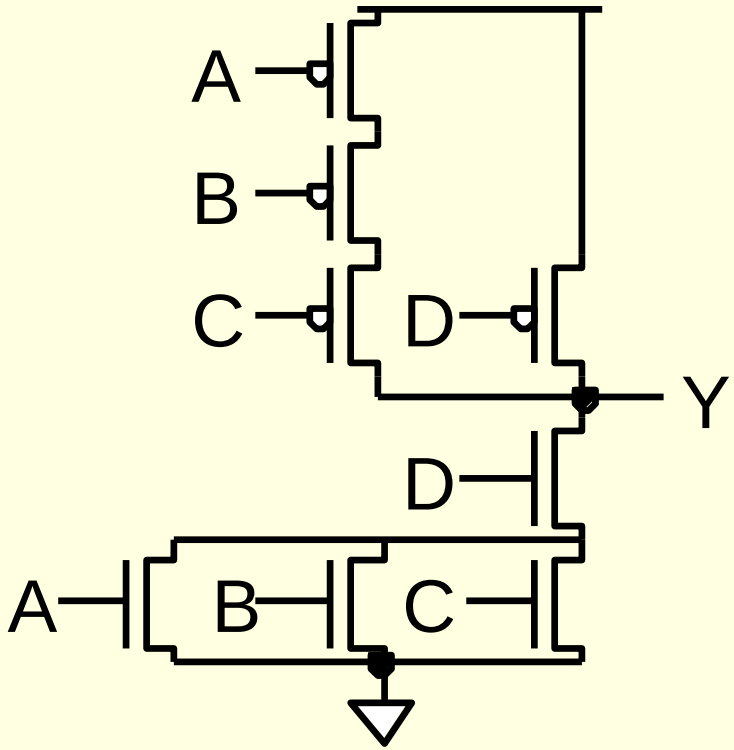


Example: O3AI

- $Y = \overline{(A + B + C) \bullet D}$

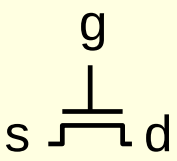
Example: O3AI

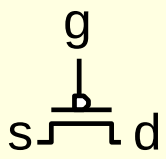
$$Y = \overline{(A + B + C) \bullet D}$$



Pass Transistors

- Transistors can be used as switches





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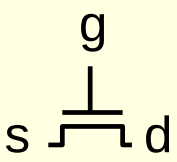

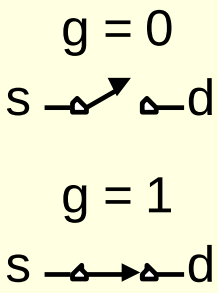

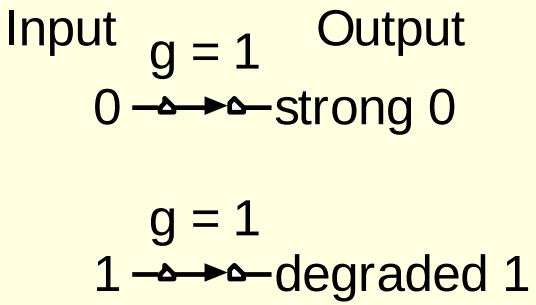

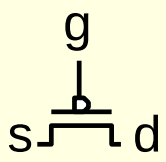

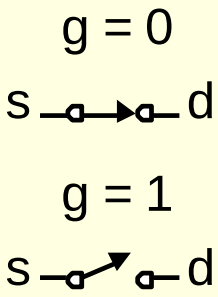

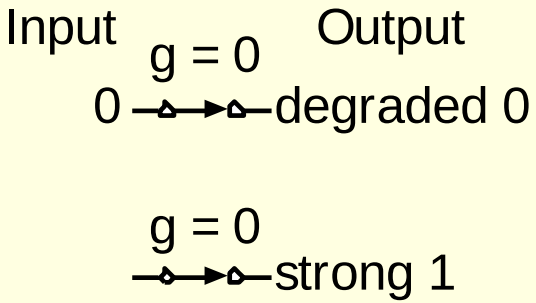

Signal Strength

- *Strength* of signal
  - How close it approximates ideal voltage source
- V_{DD} and GND rails are strongest 1 and 0
- nMOS pass strong 0
  - But degraded or weak 1
- pMOS pass strong 1
  - But degraded or weak 0
- Thus NMOS are best for pull-down network
- Thus PMOS are best for pull-up network

Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

Transmission Gates

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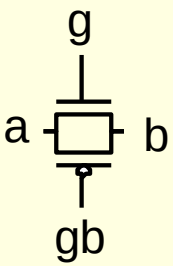
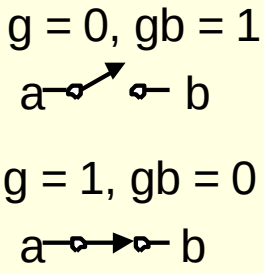
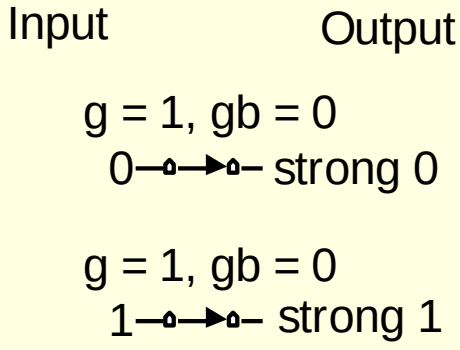
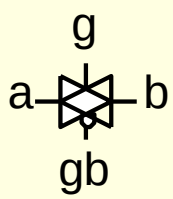
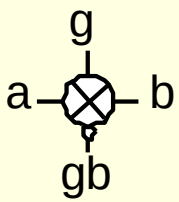
- *Transmission gates* pass both 0 and 1 well

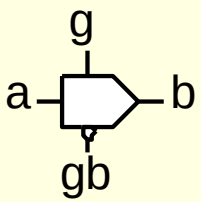












END OF LECTURE 1