ECE 211 Electronics 2

First Term 2024

Dr. Rania Fuoad Ahmed

Textbook and References

- A. Sedra and W. Smith, Microelectronic Circuits. 5th edition.
- Fundamentals of Microelectronics Second Edition Behzad Razavi (Text Book)

References of Lecture Notes

- Lecture Notes of Prof. Dr. : Dr. Rania A. Abul-Souad
- Lecture Notes of the text book: “Fundamentals of Microelectronics, Second Edition, BehzadRazavi
- Lecture Notes of Prof. Dr. Mohamed Dosoky, Ein-Shams University

Administrative rules

- Course schedule
- Lecture : Sunday (1st slot), 8:00-10:00
- Teaching assistant: Eng. Shymaa Emad

☐Grading Policy

- Assignments: 5
- Quizzes: 10
- Mid term exam: 20
- Oral exam: 15
- Final exam: 75

Course Outlines

date	subject
29/9/2024 (week 1)	Lecture 1 review of first stage
13/10/2024 (week 3)	Lecture 2 multistage amplifiers
20/10/2024 (week 4)	Lecture 3 current mirrors
27/10/2024 (week 5)	Lecture 4 cascode amplifiers
3/11/2024 (week 6)	Lecture 5 frequency response
10/11/2024 (week 7)	Lecture 6 frequency response (Cont.)
17/11/2024 (week 8)	Midterm
24/11/2024 (week 9)	Lecture 7 feedback amplifiers
1/12/2024 (week 10)	Lecture 8 feedback amplifiers (Cont.)
8/12/2024 (week 11)	Lecture 9 power amplifiers
15/12/2024 (week 12)	Lecture 10 power amplifiers (Cont.)
22/12/2024 (week 13)	Lecture 11 review

MOS Amplifiers – Biasing

- Get transistor I_D, V_{GS}, V_{DS}
- Solve input and output loops KVL
- I_G = 0 simplifies the analysis
- We have

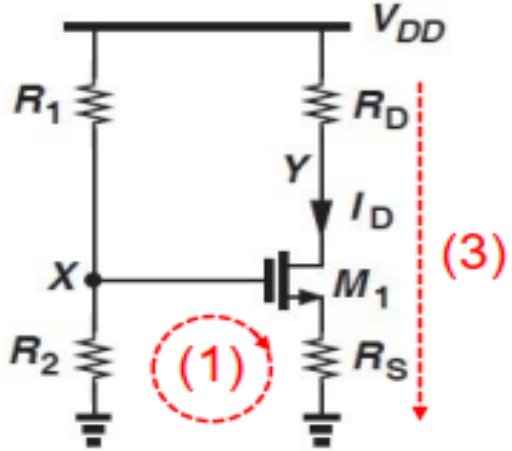
$$V_X = \frac{R_2}{R_1 + R_2} V_{DD}$$

- So we can write

$$\frac{R_2}{R_1 + R_2} V_{DD} = V_{GS} + I_D R_S \qquad (1)$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \qquad (2)$$

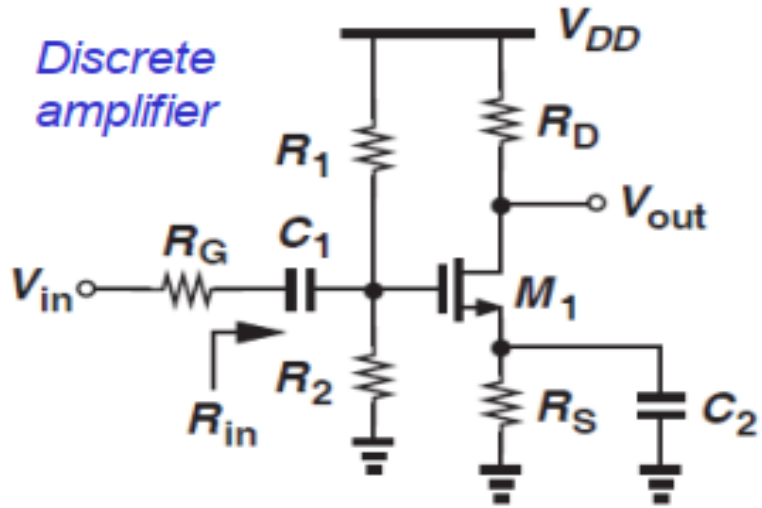
- Solve to get V_{GS} and I_D
- Then solve the output loop to get V_{DS} (3)
- V_{TH}, μ_n, C_{ox} are technology parameters and not design parameters.



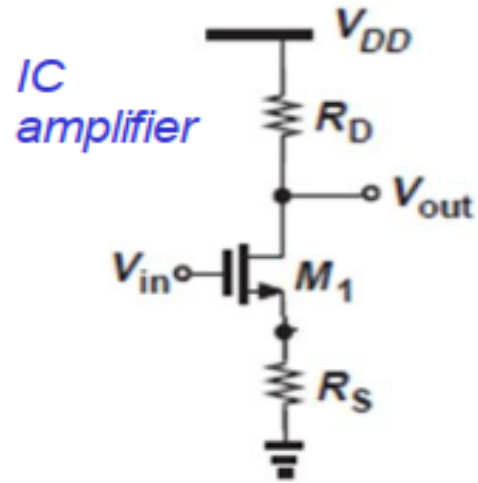
MOS transistor Biasing

Common-Source (CS) Stage – Biasing

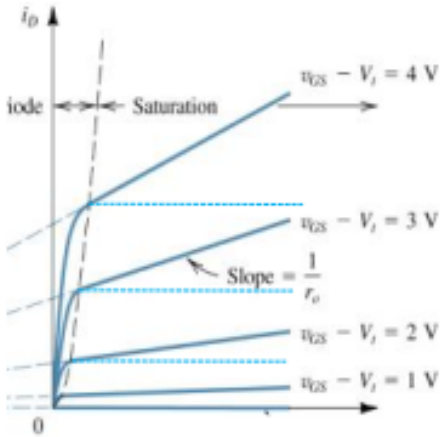
- Similar to common-emitter biasing.
- This is typical biasing in **discrete implementations**.
- R_1 and R_2 set gate voltage.
- C_1 decouples any dc voltage from previous stages.
- But the bias current depends on V_{DD}!!
- What about battery-operated systems?

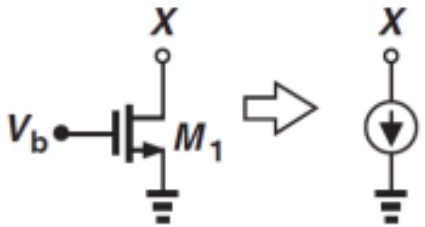


- In **IC realization**, usually the cascaded stages are designed such that the output dc bias from a stage is appropriate for biasing the next stage.
- Avoid large caps and resistors to save the valuable chip area.
- Can we achieve bias insensitivity to V_{DD}?

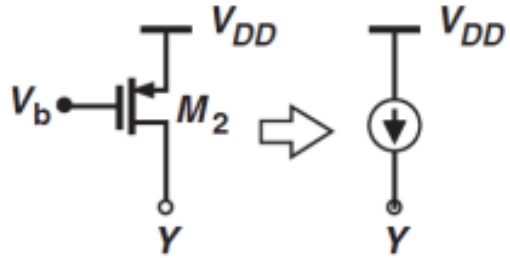


Biasing with Current Sources in ICs

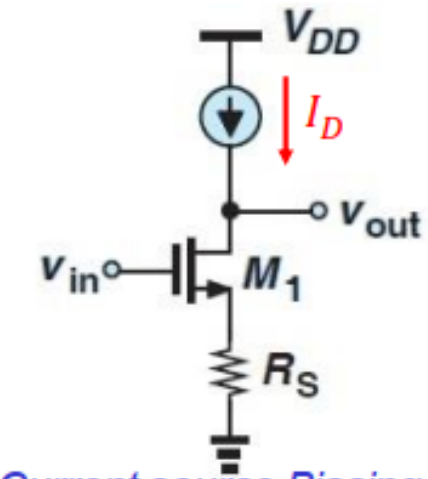




NMOS current sink



PMOS current source



Current source Biasing

- MOSFET in saturation approaches a current source.
- Current sources need a constant bias voltage V_b
- In IC design, it is possible to generate constant bias voltages, V_b, independent of V_{DD} and temperature, using circuits known as **Bandgap** circuits.
- Current source biasing is often employed in IC design.
- It sets the transistor current, and hence V_{GS}.
- Hence the bias is supply and temperature independent.

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(W/L\right)}}$$

CS Stage – Output Swing

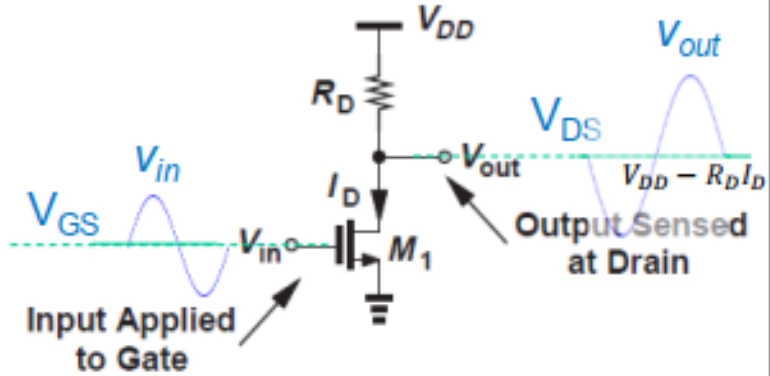
- The Transistor is biased in Saturation.
  Therefore $V_{GS} > V_{TH}$

  $$V_{DD} - R_D I_D > V_{GS} - V_{TH}$$
- The output varies around $V_{DD} - R_D I_D$
- Maximum lower excursion:

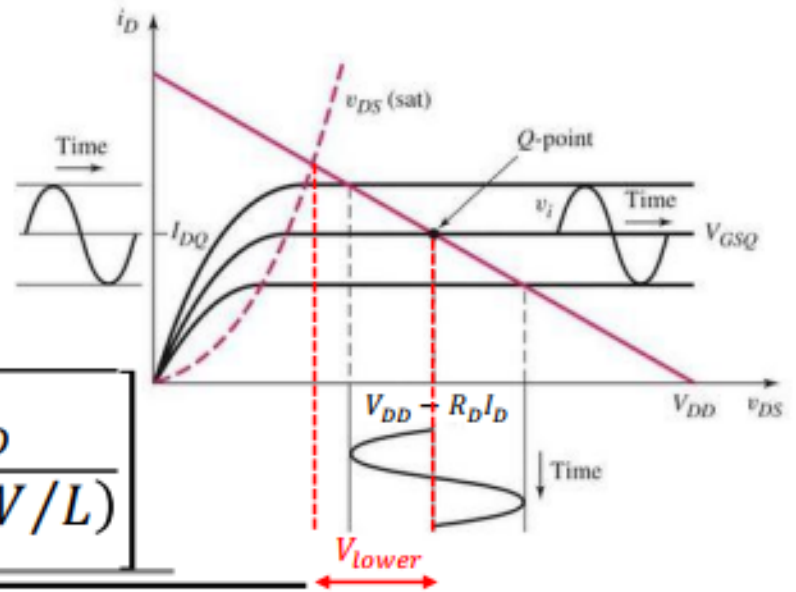
  $$V_{lower} = (V_{DD} - R_D I_D) - (V_{GS} - V_{TH})$$

  $$V_{DSsat} = V_{GS} - V_{TH} \approx \sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}}$$
- For a sine input, the output should be symmetrical around the bias point without clipping.
- To increase the swing, we should lower V_{DSsat} , *i.e.* I_D

$$V_{swing} = 2\left[(V_{DD} - R_D I_D) - \sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}}\right]$$



CS stage

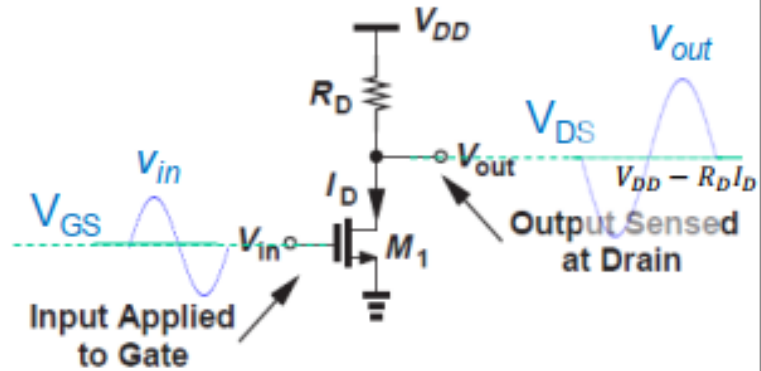


CS Stage – Gain

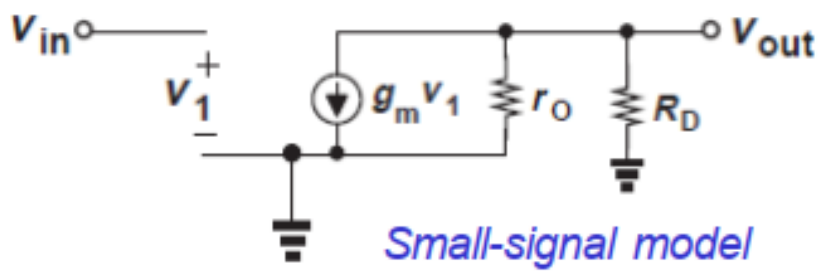
$$A_v = -g_m(R_D||r_O)$$

$$A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}(R_D||r_O)$$

- If the input *signal* goes up and down substantially, so do I_D and the gain, causing a nonlinear characteristic.
- Hence the assumption of a small-signal is important for linearity.



CS stage



Small-signal model

CS Stage – Input & Output Resistance

- Input resistance

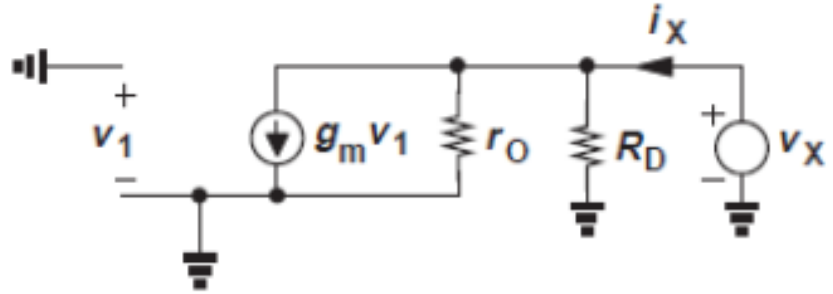
$$R_{in} = \infty$$

- Output resistance

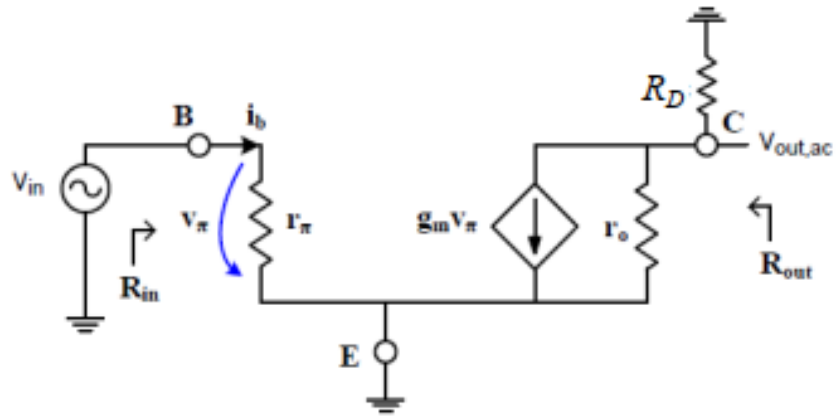
$$R_{out} = R_D || r_O.$$

- BJT Case: For common-emitter,
  - Input resistance = r_π
  - Same output resistance

- Gain $\propto R_{out}$
- r_o is usually a high resistance
- Gain is limited by R_D

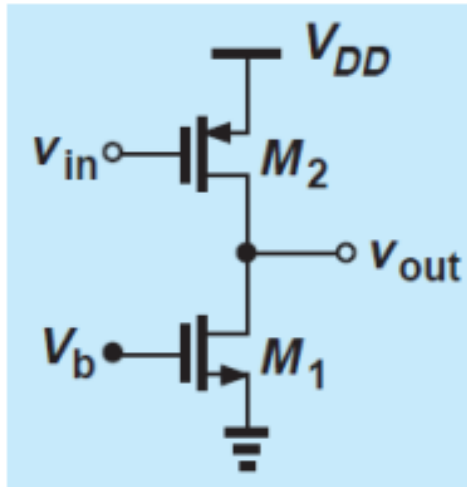


CS small-signal model



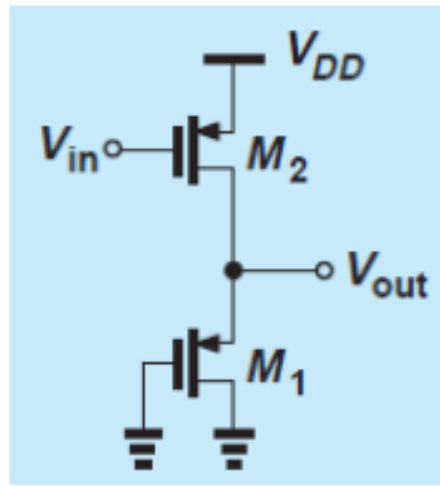
CE small-signal model

Example 1



Signal transistor
= PMOS amplifier

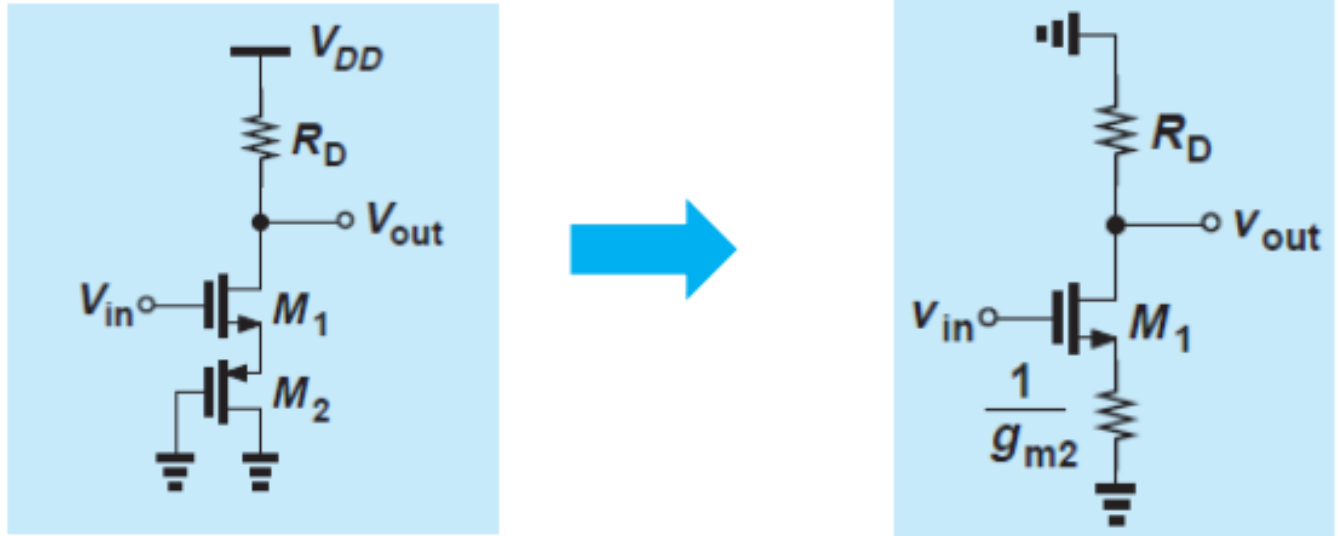
Constant gate voltage
= current source



CS $A_v = -g_m(R_D||r_O)$ **CS**

$$A_v = -g_{m2}(r_{O1}||r_{O2}) \qquad A_v \approx -\frac{g_{m2}}{g_{m1}}$$

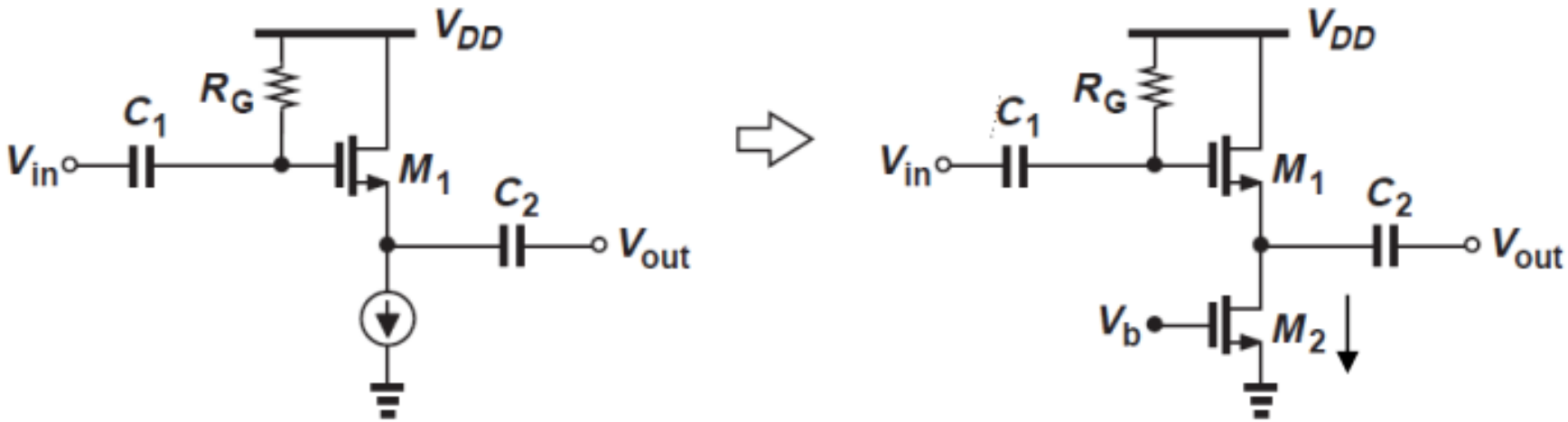
Example 2



CS *w.* degeneration

$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

Common Drain (CD) Stage – Biasing



CD stage bias with current source

- In IC design a current source is used for biasing the main transistor.
- The current sets the bias point and hence V_{GS}

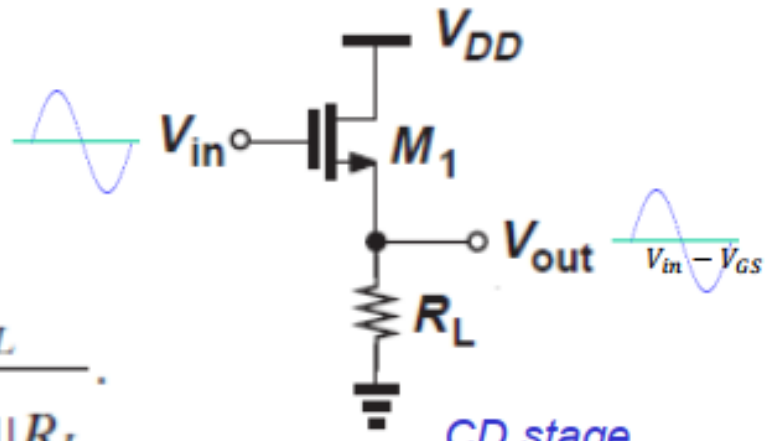
$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{TH}$$

CD Stage – Gain

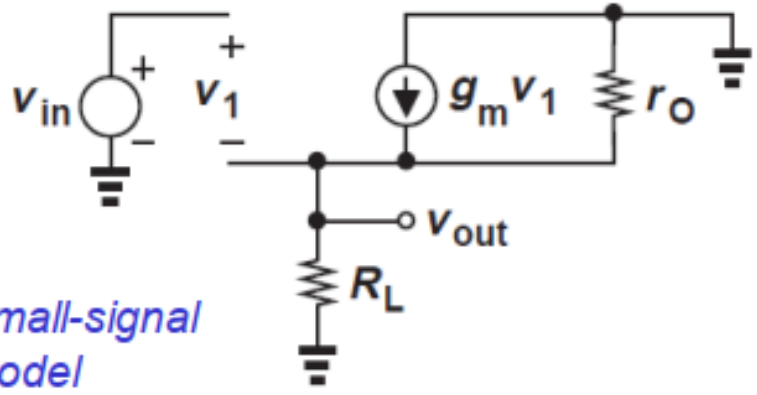
$$g_m v_1 (r_O || R_L) = v_{out}$$

$$v_{in} = v_1 + v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m (r_O || R_L)}{1 + g_m (r_O || R_L)} = \frac{r_O || R_L}{\frac{1}{g_m} + r_O || R_L}.$$



- Gain is lower than unity!!
- Approaches unity as $g_m (r_O || R_L)$ is increased.



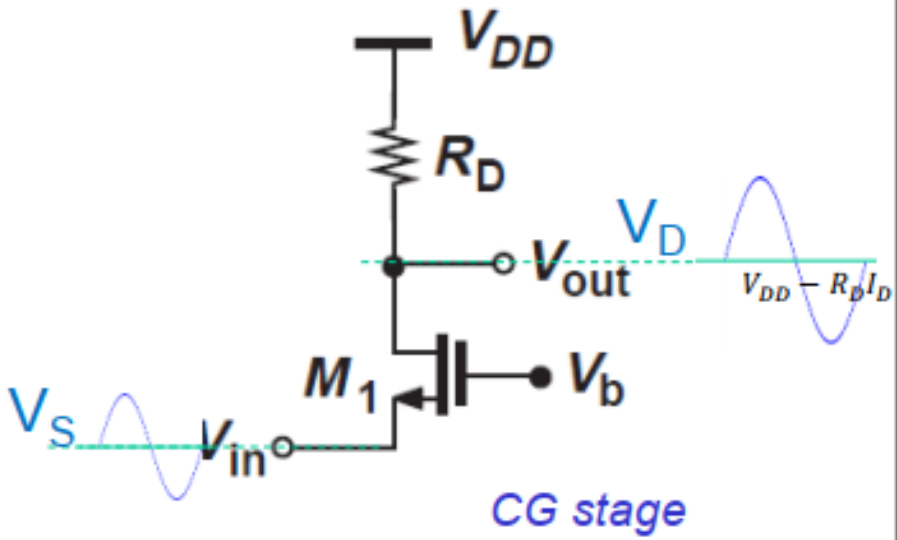
CG Stage – Gain

- Same voltage gain as CS stage, but positive.

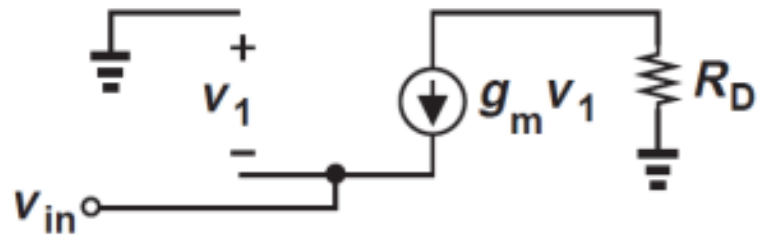
$$A_v = g_m R_D$$

- Same CS design trade-offs.

- For high gain, a high R_D is necessary,
- M_1 to remain in saturation:
  $V_{DD} - I_D R_D > V_b - V_{TH}$



CG stage

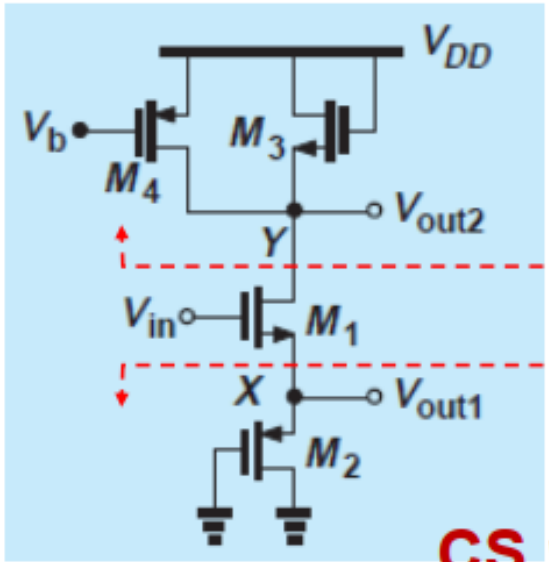


Small-signal model

Example 1

Transistors

- M_1: Amplifier
- M_2: Diode-connected
- M_3: Diode-connected
- M_4: Current Source



$$\frac{1}{g_{m3}}||r_{O3}||r_{O4}$$

$$\frac{1}{g_{m2}}||r_{O2}$$

$r_{O1} = \infty$

Source Follower

CS *w.* degeneration

$$\frac{v_{out1}}{v_{in}} = \frac{\frac{1}{g_{m2}}||r_{O2}}{\frac{1}{g_{m2}}||r_{O2} + \frac{1}{g_{m1}}} \approx \frac{g_{m1}}{g_{m1} + g_{m2}}$$

$$\frac{v_{out2}}{v_{in}} = -\frac{\frac{1}{g_{m3}}||r_{O3}||r_{O4}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}||r_{O2}} \approx -\frac{1/g_{m3}}{1/g_{m1} + 1/g_{m2}}$$

Valid since $r_{O1} = \infty$

END OF LECTURE 1