Electronics 4
Third Year

Dr. Rania Fouad Ahmed

First Term

2023-2024

References of Lecture Notes

- Prof. Dr. Soliman Mahmoud Lecture notes
- Prpf. Dr. Ahmed Nader Lecture Notes
- Prof. Dr. Razavi Lecture notes

Administrative rules

Course schedule

- Lecture : Sunday (2nd slot),
- Teaching assistant: Eng. Shymaa Emad

☐ Grading Policy

- Assignments and attendance: 10
- Quizzes: 10
- Mid term exam: 20,
- Oral exam:20
- Final exam: 90

Course Outlines

date	subject
29/9/2024 (week 1)	Lecture 1 comparator circuits
13/10/2024 (week 3)	Lecture 2 analog multipliers
20/10/2024 (week 4)	Lecture 3 analog multipliers (Cont.)
27/10/2024 (week 5)	Lecture 4 opamp non-linear applications
3/11/2024 (week 6)	Lecture 5 voltage and current reference circuits
10/11/2024 (week 7)	Lecture 6 oscillators
17/11/2024 (week 8)	Midterm
24/11/2024 (week 9)	Lecture 7 oscillators (Cont.)
1/12/2024 (week 10)	Lecture 8 analog conditioning
8/12/2024 (week 11)	Lecture 9 CFOA active block
15/12/2024 (week 12)	Lecture 10 transconductance active block
22/12/2024 (week 13)	Lecture 11 review

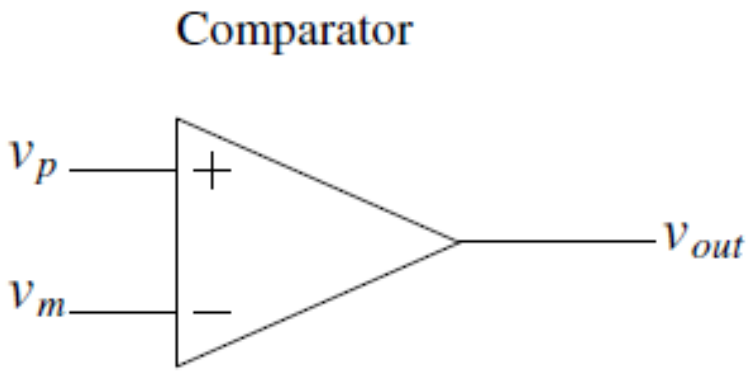
Text Book and References

- ***CMOS circuit design, layout and simulation***, *Fourth Edition by R. Jacob Baker*
- ***RF MICROELECTRONICS***, *Second Edition by Behzad Razavi*
- ***Design of Analog CMOS Integrated Circuits***, *second Edition, by Behzad Razavi*

Nonlinear Analog Circuits

- *nonlinear analog circuits:* the inputs are not linearly related to the outputs.
- In particular, we discuss **voltage comparator** analysis and design, adaptive biasing
- and **analog multiplier** design.

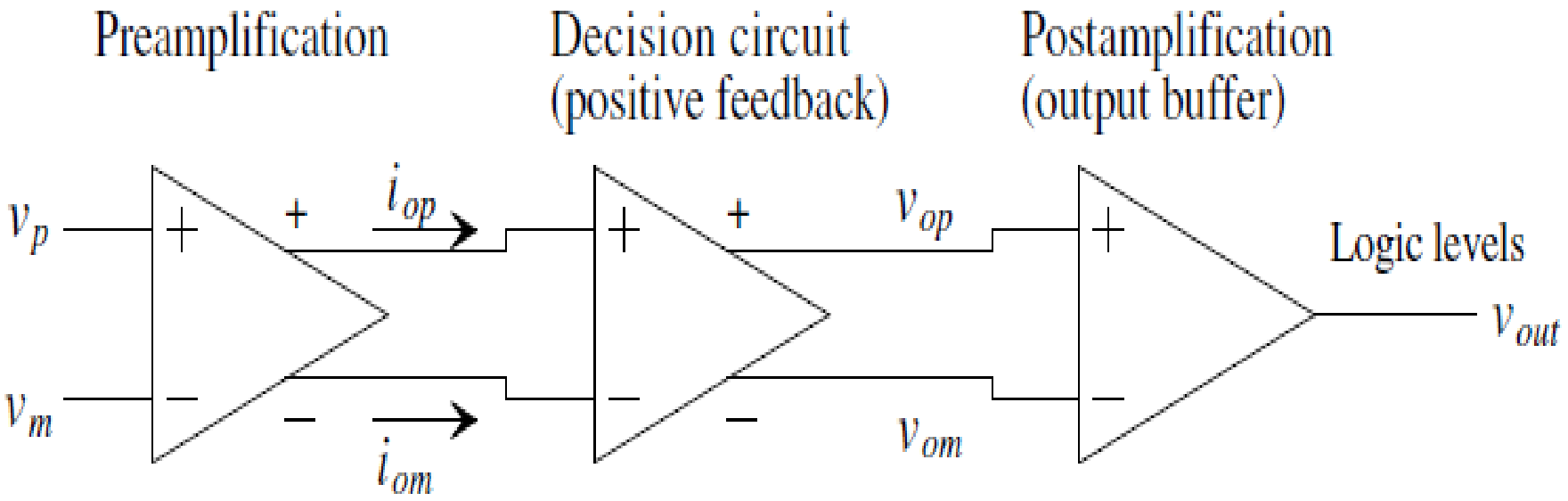
Basic CMOS Comparator Design



$v_p > v_m$ then $v_{out} = VDD$ = logic 1

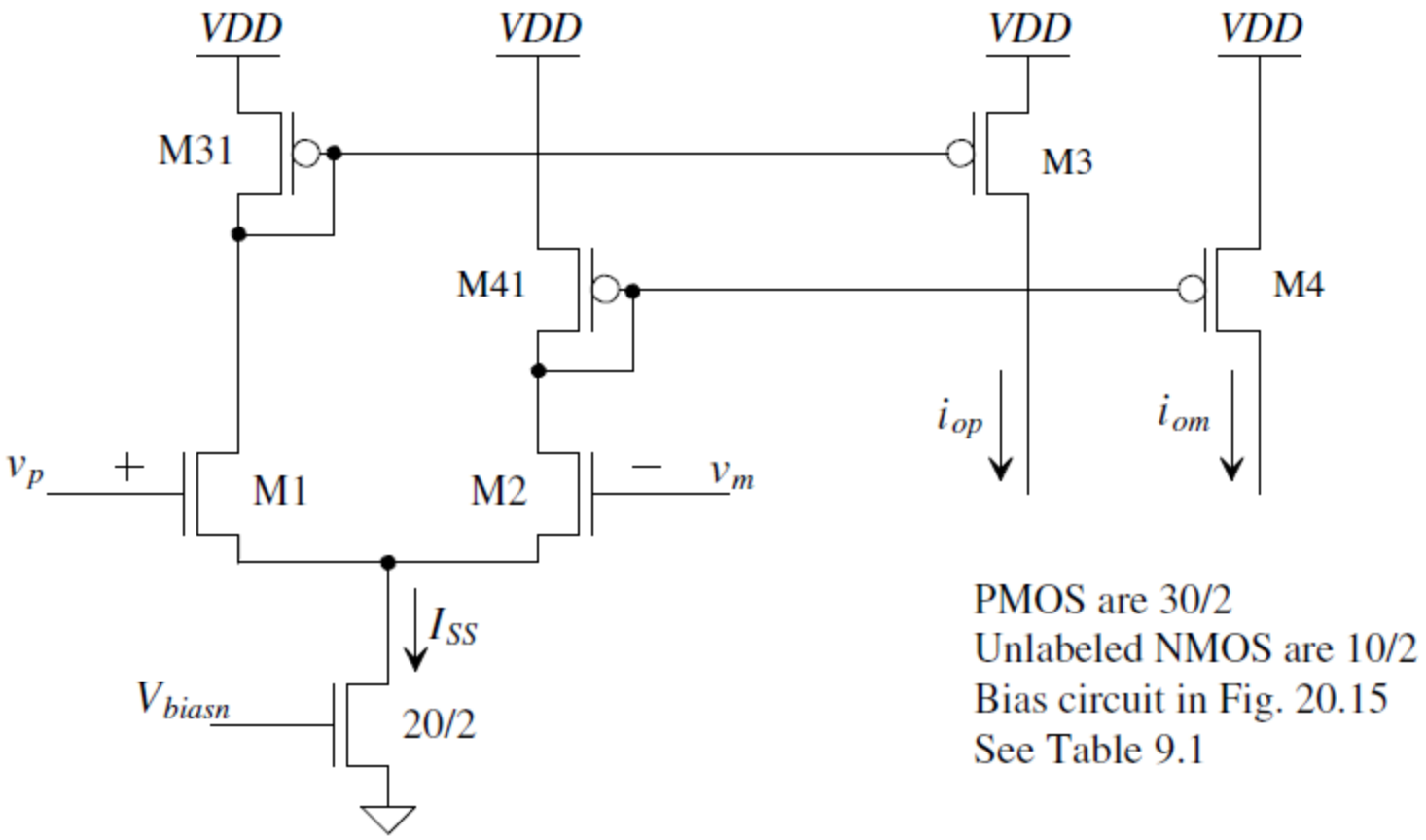
$v_p < v_m$ then $v_{out} = 0$ = logic 0

Block diagram of a voltage comparator



- The comparator consists of three stages: the input preamplifier, a positive feedback or decision stage, and an output buffer.
- The pre-amp stage: amplifies the input signal to improve the comparator sensitivity (i.e., increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage.
- The positive feedback stage: determines which of the input signals is larger.
- The output buffer: amplifies this information and outputs a digital signal.
- Designing a comparator can begin with considering input common-mode range, power dissipation, propagation delay, and comparator gain.

Preamplification stage of comparator

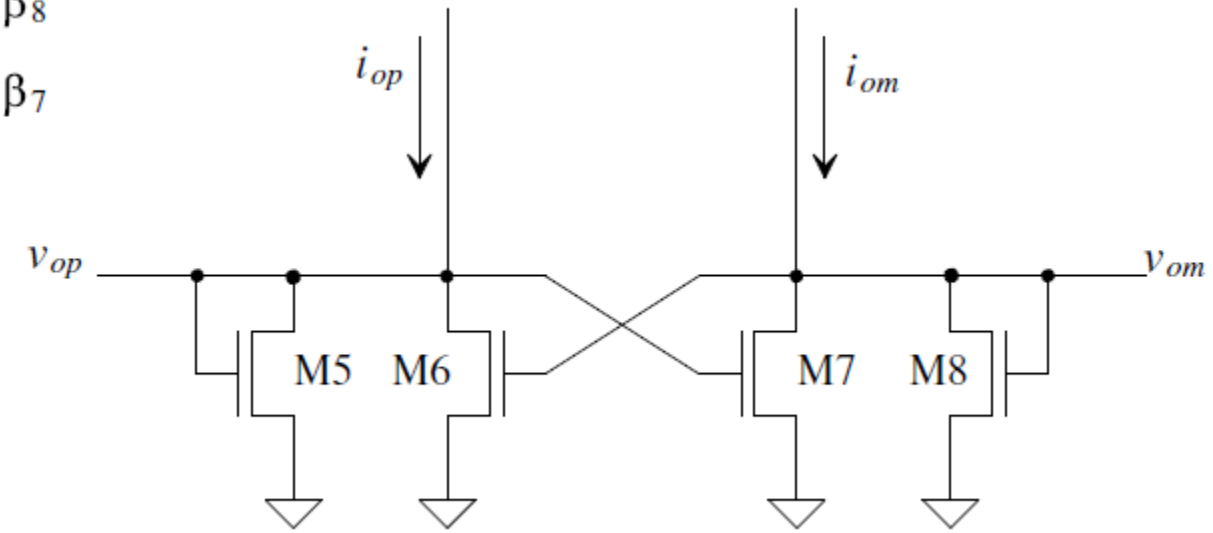


$$i_{op} = \frac{g_m}{2}(v_p - v_m) + \frac{I_{SS}}{2} = I_{SS} - i_{om}$$

Positive feedback decision circuit

$\beta_A = \beta_5 = \beta_8$

$\beta_B = \beta_6 = \beta_7$



Let's begin by assuming that i_{op} is much larger than i_{om}

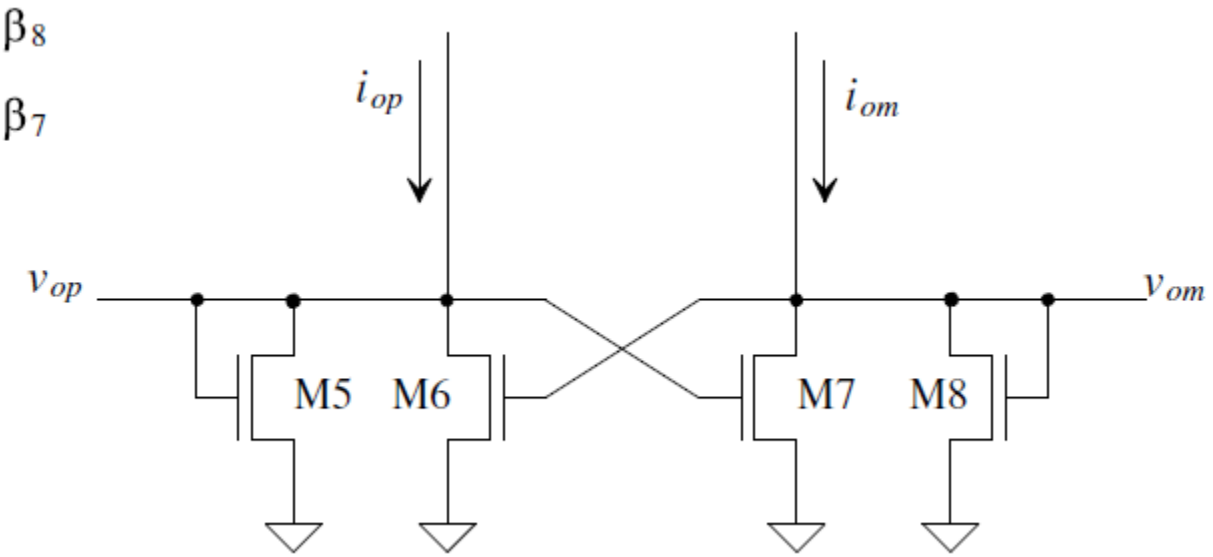
M5 and M7 are on and M6 and M8 are off

v_{om} is approximately 0 V

$$v_{op} = \sqrt{\frac{2i_{op}}{\beta_A}} + V_{THN}$$

$\beta_A = \beta_5 = \beta_8$

$\beta_B = \beta_6 = \beta_7$



When M8 is just about to turn on (M8's V_{GS} is approaching V_{THN} but the drain currents of M8 and M6 are still zero), the current flowing in M7 is

$$i_{om} = \frac{\beta_B}{2}(v_{op} - V_{THN})^2$$

and the current flowing in M5 is

$$i_{op} = \frac{\beta_A}{2}(v_{op} - V_{THN})^2$$

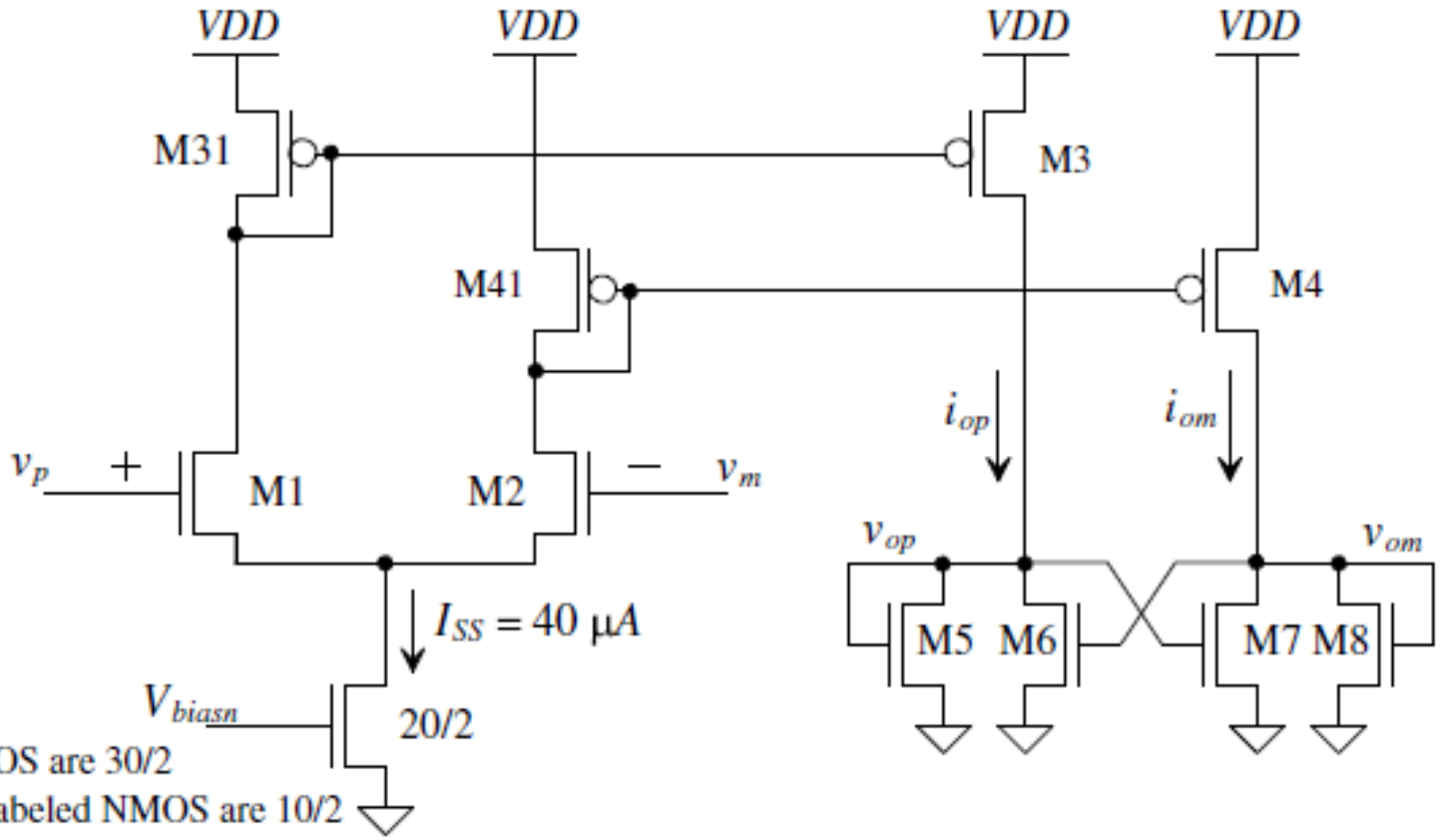
$$i_{op} = \frac{\beta_A}{\beta_B} \cdot i_{om}$$

If $\beta_A = \beta_B$, then switching takes place when the currents, i_{op} and i_{om}, are equal. Unequal βs cause the comparator to exhibit hysteresis. the switching point voltages:

$$V_{SPH} = v_p - v_m = \frac{I_{SS}}{g_m} \cdot \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} \text{ for } \beta_B \geq \beta_A$$

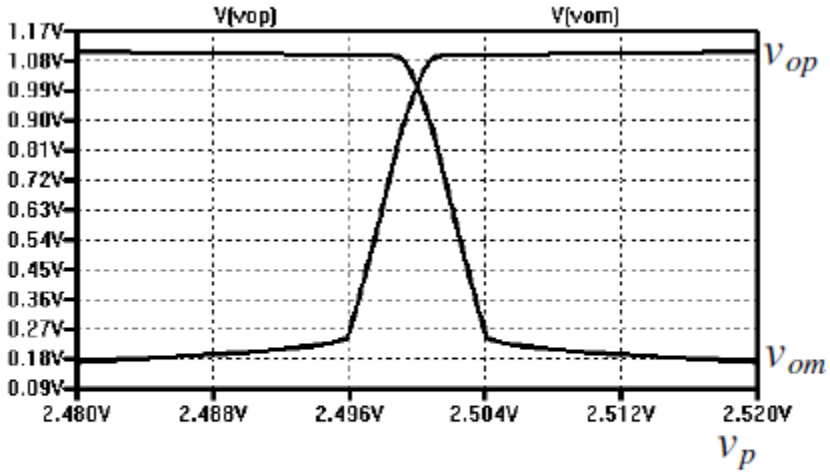
Example 27.1

For the circuit shown in Fig. 27.5, estimate and simulate the switching point voltages for two designs: (1) $W_5 = W_6 = W_7 = W_8 = 10$ with $L = 1$ and (2) $W_5 = W_8 = 10$ and $W_6 = W_7 = 12$ with $L = 1$.

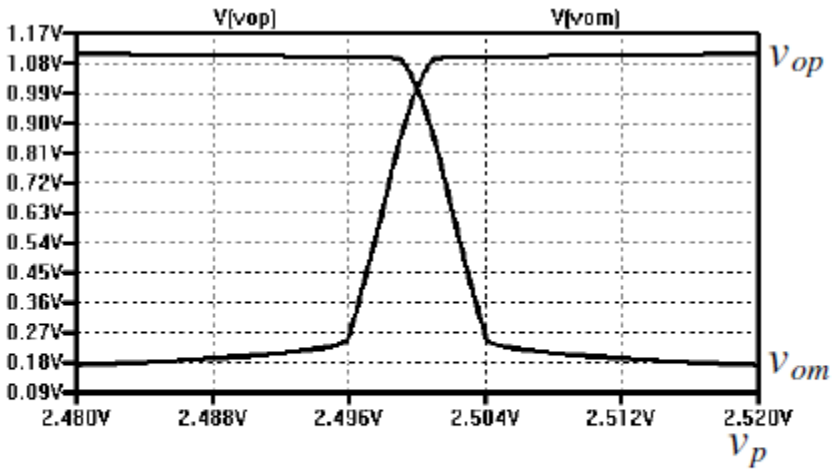


$$\beta_A = \beta_B = 120\,\frac{\mu A}{V^2}\cdot\frac{10}{1} = 1.2\ mA/V^2$$

$$V_{SPH} = V_{SPL} = 0.$$



(a) Minus input held at 2.5 V while the positive input is swept from 2.48 to 2.52 V.



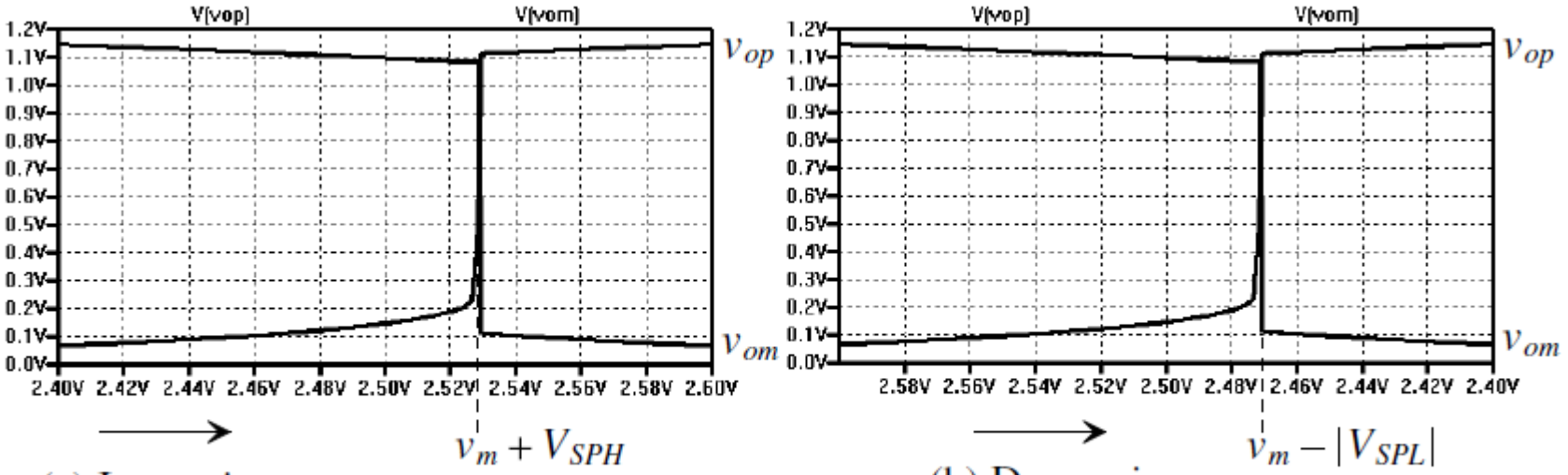
(b) Minus input held at 2.5 V while the positive input is swept from 2.52 to 2.48.

For the second case

$$\beta_A = 120\,\frac{\mu A}{V^2}\cdot\frac{10}{1} \text{ and } \beta_B = 120\,\frac{\mu A}{V^2}\cdot\frac{12}{1}$$

with $I_{SS} = 40\ \mu\text{A}$ and $g_m = 150\ \mu\text{A/V}$

$$V_{SPH} = -V_{SPL} = \frac{I_{SS}}{g_m}\cdot\frac{\frac{\beta_B}{\beta_A}-1}{\frac{\beta_B}{\beta_A}+1} = \frac{40}{150}\cdot\frac{1.2-1}{1.2+1} = 24\ mV$$

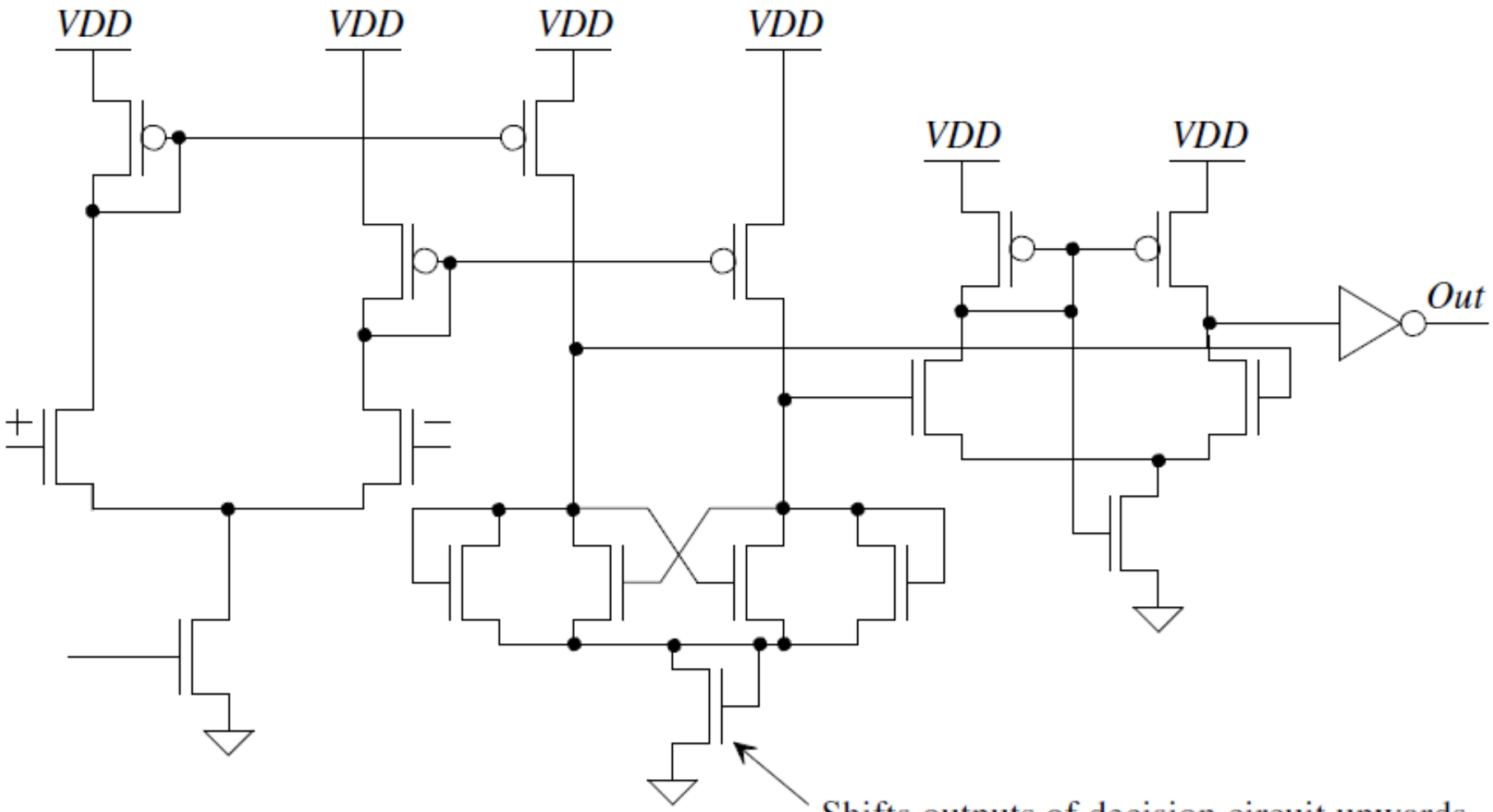


(a) Increasing v_p $\qquad v_m = 2.5\ V$ $\qquad$ (b) Decreasing v_p

Output Buffer

- The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or *VDD*).

Using a self-biased diff-amp for the output buffer



End of Lecture 1